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DATE MAILED: 02/08/96

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

☑ This application has been examined   ☐ Responsive to communication filed on _____   ☐ This action is made final.

A shortened statutory period for response to this action is set to expire __3__ month(s), __0__ days from the date of this letter.
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I   THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☑ Notice of References Cited by Examiner, PTO-892.   2. ☐ Notice of Draftsman's Patent Drawing Review, PTO-948.
3. ☑ Notice of Art Cited by Applicant, PTO-1449.   4. ☐ Notice of Informal Patent Application, PTO-152.
5. ☐ Information on How to Effect Drawing Changes, PTO-1474.   6. ☐ _____

Part II   SUMMARY OF ACTION

1. ☑ Claims _1—18_ _____ are pending in the application.

   Of the above, claims _____ are withdrawn from consideration.

2. ☐ Claims _____ have been cancelled.

3. ☐ Claims _____ are allowed.

4. ☑ Claims _1—18_ _____ are rejected.

5. ☐ Claims _____ are objected to.

6. ☐ Claims _____ are subject to restriction or election requirement.

7. ☐ This application has been filed with informal drawings under 37 C.F.R. 1.85 which are acceptable for examination purposes.

8. ☐ Formal drawings are required in response to this Office action.

9. ☐ The corrected or substitute drawings have been received on _____. Under 37 C.F.R. 1.84 these drawings
   are ☐ acceptable; ☐ not acceptable (see explanation or Notice of Draftsman's Patent Drawing Review, PTO-948).

10. ☐ The proposed additional or substitute sheet(s) of drawings, filed on _____. has (have) been ☐ approved by the
   examiner; ☐ disapproved by the examiner (see explanation).

11. ☐ The proposed drawing correction, filed _____, has been ☐ approved; ☐ disapproved (see explanation).

12. ☐ Acknowledgement is made of the claim for priority under 35 U.S.C. 119. The certified copy has ☐ been received ☐ not been received
   ☐ been filed in parent application, serial no. _____ ; filed on _____.

13. ☐ Since this application apppears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in
   accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.

14. ☐ Other

Part III   DETAILED ACTION

Priority

1.   Receipt is acknowledged of papers submitted under 35 U.S.C. § 119, which papers

have been placed of record in the file.

Drawings

2.   This application has been filed with informal drawings which are acceptable for

examination purposes only. Formal drawings will be required when the application is

allowed.

Claim Rejections - 35 USC § 112

3.   Claim 9 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for

failing to particularly point out and distinctly claim the subject matter which applicant

regards as the invention. The claim is indefinite because it is unclear what the applicant

meant by the phrase "wherein the cache replacement mechanism transfer a sector from the

storage element to the cache memory when a read or write request has given rise to the

sector being read from the storage element responsive to the sector being access on the most

recent one or more occasions." More particularly, since the first part of the claim implies that

the cache only maintains historical information on entries within cache, it is unclear as to

how the replacement mechanism would base its decision to transfer the sector from the

storage element to the cache based on that sector being accessed on the "most recent one or

more occasions."

Claim Rejections - 35 USC § 102

4.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that
form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a
foreign country or in public use or on sale in this country, more than one year prior
to the date of application for patent in the United States.

5.   Claims 1, 2 and 18 are rejected under 35 U.S.C. § 102(b) as being anticipated by

Yamazaki, *et al*, (Japanese Patent Application laid open 4-205852.)

As to claim 1:

(a)   Yamazaki teaches a solid state cache memory. For example, Fig. 2, element 204 shows

a cache memory. Yamazaki inherently teaches that the cache memory is solid state

technology because caches are typically made using solid technologies.

(b)   Yamazaki teaches a storage element with at least one moving part where in the

storage element has an operating mode, and a non fully operating mode when data access

has not occurred for a predetermined time period. Yamazaki teaches the use of a disk drive,

which has at least one moving part (*e.g.*: the disk platters, or disk head assembly, motor,

spindle, *etc.*) Yamazaki also teaches that the storage element has both an operating mode and

a non fully operating mode when data access has not occurred for a predetermined period of time. On pp. 4-5 of the translation, and referring to Fig. 1, Yamazaki teaches that the disk's motor is powered on at step 17, the data transfer occurs at step 18, and the disk's motor is powered off at step 19. The process of powering the disk motor on and off constitute the fully operating mode and the non fully operating mode. The amount of time which elapses between data access and the initiation of the non fully operating mode is predetermined because it is equal to the time it takes the necessary circuitry to detect that the disk has finished servicing a data access request plus the time it takes to switch off the motor.

(c)   Yamazaki also teaches the use of a cache control system as claimed. On page 5 of the translation, Yamazaki teaches that the cache control system is responsive to read and write requests from the computer because if a requested disk transaction results in a cache hit, the transaction is satisfied via the cache memory. Similarly, Yamazaki also teaches that in the event of a cache miss, data is transferred from the disk to the cache, and then to the computer. This is both the claimed means to access the data as well as the claimed cache replacement mechanism. Note too that Yamazaki also teaches that data transfers are not performed to the disk until it reaches operating speed because Yamazaki teaches at step 17 that disk motor is turned on before the data transfer. Finally, Yamazaki inherently teaches a cache which maintains data consistency because a consistency is required in order for a cache to be useful.

As to claim 2:

In addition to the foregoing, Yamazaki also inherently teaches that the cache replacement

mechanism carries out transfers from cache to the storage element for a predetermined time

each time a read or write request gives rise to an access to the storage element because

caches are typically organized into equal lines which are flushed as an unit. Because each line

is the same size, the time it takes to flush a line is predetermined.

As to claim 18:

This claim is a method claim which parallels the apparatus claim of claim 1. Therefore, claim

18 is rejected for the same reasons as claim 1.

Claim Rejections - 35 USC § 103

6.   The following is a quotation of 35 U.S.C. § 103 which forms the basis for all
obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or
> described as set forth in section 102 of this title, if the differences between the subject
> matter sought to be patented and the prior art are such that the subject matter as a
> whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability
> shall not be negatived by the manner in which the invention was made.
>
> Subject matter developed by another person, which qualifies as prior art only under
> subsection (f) or (g) of section 102 of this title, shall not preclude patentability under
> this section where the subject matter and the claimed invention were, at the time the

invention was made, owned by the same person or subject to an obligation of assignment to the same person.

7.   Claim 3 is rejected under 35 U.S.C. § 103 as being unpatentable over Yamazaki as applied to claim 1 above, and further in view of Hanson, *et al.* (US Patent 4,433,374). Yamazaki teaches every feature of the instant claim except for the cache bypass feature. See rejection of claim 1, above. Hanson teaches a cache/disk subsystem with a cache bypass feature. In particular, at col. 4, lines 60 through col. 5, line 66, Hansen teaches bypassing a disk cache for disk transactions which exceed a certain threshold. Indeed Hansen teaches that "extremely long data transfers usually involve data that is not likely to be used again soon." Col. 5, lines 1-3. It therefore would have been obvious at the time the invention was made to one of ordinary skill in the art to have combined the teachings of Yamazaki and Hansen to have arrived at the claimed invention because a cache bypass feature for large data transfers would increase the cache efficiency by maintaining a high cache hit ratio, since caching large transfers have been shown to be ineffective.

8.   Claim 4 is rejected under 35 U.S.C. § 103 as being unpatentable over Yamazaki as applied to claim 1 above, and further in view of Macon, *et. al* (US Patent No. 5,410,653). Yamazaki teaches every element claim 1. Claim 4 differs from claim 1 by further requiring that the data be stored in sectors, and each sector has a set of sectors associated with it, and that the cache replacement mechanism transfers all members of the set into the cache when a read/write request causes a sector to be read from the storage element.

Macon teaches the use of sector organized storage since disks are normally organized by

sectors. In the terminology of Macon, sectors are called blocks. *See* Macon, col. 1, 14-30.

Macon also teaches the identification of a set of sectors associated with a particular sector,

and the reading of the set of associated set of sectors if the sector in question needs to be

transferred from the disk to the cache because the read ahead would eliminate the need of

future disk access. Macon, col. 1, 14-46 and col. 2, 13-29. Macon does not teach the transfer of

the associated set of sectors if the sector in question is written from the cache to the disk,

however, such an operation is logically equivalent to reading the same sector from the disk.

It therefore would have been obvious at the time the invention was made to one of ordinary

skill in the art to have combined the teachings of Yamazaki and Macon, and to extend the

same to include both reading and writing because transferring the set of sectors would

improve efficiency.

9.   Claims 5 and 6 are rejected under 35 U.S.C. § 103 as being unpatentable over

Yamazaki as applied to claim 1 above, and further in view of a book entitled *Computer*

Networks by Andrew Tanebaum (1st Edition, (C) 1981, ISBN 0-13-165183-8), hereinafter

Tanebaum. Claims 5 and 6 differ from claim 1 by, *inter alia*, containing a restriction that dirty

cache entries are not flushed to disk until a disk transaction which would cause disk action

occurs. Claim 6 differs from claim 5 by further limiting the order in which dirty cache entries

are flush in a FIFO manner. In addition to teaching every element of claim 1, Yamazaki also

inherently teaches the means for identifying sectors in the cache which contain information

fresher than the corresponding sectors in the storage element because any disk cache may

operate in write-back mode, and any such cache must be able to identify dirty data in order

to maintain consistency. Yamazaki, however, does not teach the delaying of write-back

operations until a read or write request forces an access to the disk.

As to claim 5:

Tanebaum, at pages 148-9 discusses a concept known as piggybacking in the context of

sliding window protocols. In particular, Tanebaum states that piggybacking is "the technique

of temporarily delaying outgoing acknowledgements so that they can be hooked onto the

next outgoing data frame", and that piggybacking achieves a more efficient use of available

bandwidth when compared against the use of separate packets to signal acknowledgement.

Although Tanebaum discusses computer networks, his situation is similar to that of the

instant invention. For example, both a computer network and the instant invention involve

sending data between two nodes. In the computer network, the data is sent from a source

computer to a destination computer. In the instant invention, data is sent from the cache to

the disk drive. In both situations, the available channel bandwidth should be conserved.

Indeed, the connection between the cache and the disk drive itself can be viewed as a *de

minimus* network. Piggybacking in a computer network protocol conserves channel

bandwidth by delaying outgoing acknowledgement packets by combining such

acknowledgements with regular outgoing traffic. Similarly, in the instant invention, the

flushing of dirty cache entries are delayed and combined with read/write traffic which

involve disk access. Therefore, it would have been obvious at the time the invention was

made to one of ordinary skill in the art to have combined the teachings of Yamazaki and

Tanebaum to arrive at the claimed invention.

As to claim 6:

Claim 6 contains the additional limitation that sectors are transferred in non-increasing order

of current time minus the most recent time that any sector in the group of sectors associated

with the sector was accessed, which is equivalent to stating that the older dirty entries are

flushed before younger dirty entries. In addition to the foregoing, Tanenbaum at pages 153-6

describes a pipelined protocol where a sender on a network may continue to send new

packets despite the lack of several acknowledgement packets. In particular, Tanebaum states

at page 154 that pipeline may result in increased efficiency. Note that a pipelined protocol

always results in the older outstanding acknowledgement packet arriving before younger

packets. This is similar to the claimed invention, where, using the analogy stated in claim 5,

the flushing of dirty cache entries is similar to the transmission of acknowledgment packets

(in a piggybacked manner). Therefore, it would have been obvious at the time the invention

was made to one of ordinary skill in the art to have combined the teachings of Yamazaki and

Tanebaum to arrive at the claimed invention.

10.   Claims 7 and 8 are rejected under 35 U.S.C. § 103 as being unpatentable over

Yamazaki and Macon as applied to claim 4 above, and further in view of Shih *et al* (US

Patent No. 5,293,609).

Claim 7 differs from claim 4 by further requiring an identification of sectors which have been

accessed in a predetermined time period and a means to update the set of associated sectors

based on a historical reference. Claim 8 differs from claim 7 by further requiring the removal

of non-accessed sectors from the set after a predetermined period of time.

As to claim 7:

Shih teaches a cache management system which automatically sizes the portions of the cache

utilized for demand and prefetched data based on cache hit densities. (Shih at col. 1, 59-66).

Shih teaches the use of a cache directory table in conjunction with LRU and MRU tables at

col 2, 2-22. The ability to gather and store LRU and MRU information necessarily means both

the ability to determine whether a cached sector has been accessed during a predetermined

time interval as well as maintaining historical information on each cached sector because the

only way to perform these calculations is to keep track of the order of access to each cached

sector. See also Shih at col. 3, 12-18, stating that Shih maintains historical information.

At col. 4, 41-68, Shih teaches that when the cache is full and a new block need to be placed

into the cache, the cache management system compares the demand cache hit density against

the prefetch cache hit density. If the demand cache hit ratio is greater than the prefetch cache

hit ratio, a prefetch cache entry is deleted to make space for the new block. In conjunction

with the forgoing, this feature teaches claim 7 because the deletion of the prefetch cache

entry updates (by deletion) the set of sectors in the cache associated with a particular sector.

Therefore, it would have been obvious at the time the invention was made to one of

ordinary skill in the art to have combined the teachings of Shih with Yamazaki and Macon in

order to arrive at the claimed invention because the addition of a hit density based

replacement method would improve cache efficiency.

As to claim 8:

The foregoing described every feature of claim 8 except for the fact that Shih teaches a

storage apparatus which removes the sector in question only when it is necessary to make

space for new sectors while the claim langauge describes an storage apparatus which

removes sector after a predetermined number of non-accesses. Thus, the differences between

Shih and the claim language is the difference between the use of a fixed threshold (which is

simpler, less costly and flexible) versus that of a dynamic on-demand threshold (which is

more flexible, more expensive and more complex). The tradeoff between complexity, cost

and flexibility is that which is regularly confronted by designers. It therefore would have

been obvious at the time the invention was made to one of ordinary skill in the art to have

substituted a fixed threshold system for the dynamic system taught by Shih because the

substitution would result in an less expensive system.

11.   Claims 10 and 14 are rejected under 35 U.S.C. § 103 as being unpatentable over

Yamazaki. Yamazaki teaches every element of claim 1 by using a magnetic disk drive as a

data storage apparatus. See rejection of claim 1, above. Claims 10 and 14 differ from claim 1

only by specifying the use of an optical drive and MO disk drive as the storage apparatus,

respectively. However, magnetic disks, optical drive, and MO disk drives are all well known

forms of disk based computer memories. Each of these devices comprise a rotating disk

shaped media and sensors mounted on an arm assembly for reading and/or writing the

data. Additionally, these devices may use the same computer interface, such as SCSI-2. In

other words, these devices are analogous, and differ primarily in reading/writing methods,

performance, capacity, and ability to withstand environmental stresses. Therefore, it would

have been obvious at the time the invention was made to one of ordinary skill in the art to

have substituted either optical or MO drives as the storage apparatus depending upon the

suitability of such devices to the intended application or the environment where the

computer system will be situated.

12.   Claims 11, 13, and 15 are rejected under 35 U.S.C. § 103 as being unpatentable over

Yamazaki as applied to claims 10, 12, and 14, respectively above, and further in view of art

common knowledge. Claims 11, 13, and 15 differ from their parent claims of 10, 12, and 14

by containing the additional limitation that the claimed storage subsystem be used in either a

personal computer or a portable computer. It is common knowledge that many disks,

optical, or MO storage subsystems may be used in a variety of computers, ranging, for

example, from engineering workstations to desktop PCs, to notebook and laptops, and sometimes even gaming consoles. The claimed storage subsystems has an advantage in it minimizes the use of electrical power, a goal which is both desirable in desktop PCs (where it reduces electrical utility costs) and especially in portable systems (where it would allow the portable system to run on batteries for a greater length of time). Therefore, it would have been obvious at the time the invention was made to one of ordinary skill in the art to have placed the storage subsystems claimed in claims 10, 12, and 14 into either a personal computer or a portable computer in order to optimize the use of power.

13.   Claim 16 is rejected under 35 U.S.C. § 103 as being unpatentable over Yamazaki as applied to claim 1 above, and further in view of Noya *et al* (US Patent 5,420,983). Yamazaki teaches every feature of claim 1. Claim 16 differs from claim 1 by having the additional limitation that the cache be non-volatile. Noya teaches a disk subsystem which uses non-volatile memory for a disk write cache. (Noya, col. 5, 30-40). In particular, Noya states that non volatile memory is used in the write cache to prevent any power failure related data corruption. While the present invention is not concerned with data corruption due to power failures, it is focused on minimizing the amount of electrical power consumed by the storage subsystem by inducing power failures in selected subsystems. If non-volatile memory were used for the cache, it would allow the storage subsystem to power down the cache after a period of inactivity without incurring any power penalty associated with having an empty cache, and thereby requiring new disk accesses to involve powering up the drive motor. Therefore, it would have been obvious at the time the invention was made to one of ordinary

skill in the art to have combined the teachings of Yamazaki and Noya to arrive at the

claimed invention because using nonvolatile memory as a cache would lead to additional

power savings.

14.   Claim 17 is rejected under 35 U.S.C. § 103 as being unpatentable over Yamazaki and

Noya as applied to claim 16 above, and further in view of art common knowledge.

Collectively, Yamazaki and Noya teach every feature of claim 17 except for the additional

limitation that the disk subsystem be used with a personal or portable computer. It is

common knowledge that many disks subsystems may be used in a variety of computers,

ranging, for example, from engineering workstations to desktop PCs, to notebook and

laptops. The claimed storage subsystems has an advantage in it minimizes the use of

electrical power, a goal which is both desirable in desktop PCs (where it reduces electrical

utility costs) and especially in portable systems (where it would allow the portable system to

run on batteries for a greater length of time). Therefore, it would have been obvious at the

time the invention was made to one of ordinary skill in the art to have placed the storage

subsystems as claimed in claims 16 into either a personal computer or a portable computer in

order to optimize the use of power.

Conclusion

15.   Any inquiry concerning this communication or earlier communications from the
examiner should be directed to Christopher Chow whose telephone number is (703) 308-6674.
The examiner can normally be reached on Monday through Thursday from 7:00 to 5:30.

Art Unit: 2318

If attempts to reach the examiner by telephone are unsuccessful the examiner's supervisor Tod Swann can be reached on (703) 308-7791. The fax phone number for this Group is (703) 308-5357.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-9600.

> Christopher Chow
> Patent Examiner
> Group 2300

TOD R. SWANN
SUPERVISORY PATENT EXAMINER
GROUP 2300